MZ MONOZUKURI

Create Innovate Realize

HANOI “Whiteboard” Flow
The Seed For 2.5D-IC Implementation

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The Problem

Almost Nothing Exists, the Blackboard Is… White

- The processor (xPU) is in the flux
- The memories selection is still ongoing
- The silicon interposer(s) do(es) not exist – yes, there may be more than one !
- The package selection is a far future concern

- Yet, some “drawing” is critical to plan ahead
  - Complexity prevents “napkin and pencil” approaches
  - Thousands of signals, microbumps, TSV, C4, design-rules,…

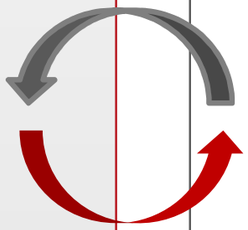
- HANOI does provide a “whiteboard” flow to the rescue
  - What exists can be imported, what doesn’t exist can be created from scratch

HANOI "Whiteboard" Flow

The Seed for 2.5D-IC Physical Implementation

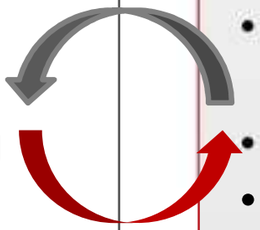
Early Exploration

- Components Import
  - HBM, Package,…
- Components Creation
  - xPU,…
- System Floorplanning
- Silicon Interposer Creation
  - TSV, C4,…
  - [Partial] Connectivity,…
- I/O Planning
- Cross-Hierarchical Optimization
- Signal Assignment
- Export to Physical Implementation



Physical Implementation (Third Party Tools)

System floorplanning
Physical Implementation
xPU,…
Silicon Interposer Routing
PHY-to-PHY
Microbump-to-TSV
TSV-to-C4



Incremental Optimization

- Import from Physical Implementation
- Components Update
  - Logical, Physical
- Silicon Interposer Update
- Incremental I/O Planning
- Incremental Optimization
- Incremental Signal Assignment
- Export to Physical Implementation

HANOI "Whiteboard" Flow

The Seed for IC Compiler Physical Implementation

Early Exploration

Hanoi

Components Import
- HBM, Package,…

- Components Creation
  - xPU,…
- System Floorplanning
- Silicon Interposer Creation
  - TSV, C4,…
  - [Partial] Connectivity,…
- I/O Planning
- Cross-Hierarchical Optimization
- Signal Assignment
- Export to Physical Implementation

Physical Implementation

IC Compiler & Custom Compiler

- System floorplanning
- Physical Implementation
  - xPU,…
- Silicon Interposer Routing
  - PHY-to-PHY
  - Microbump-to-TSV-to-C4

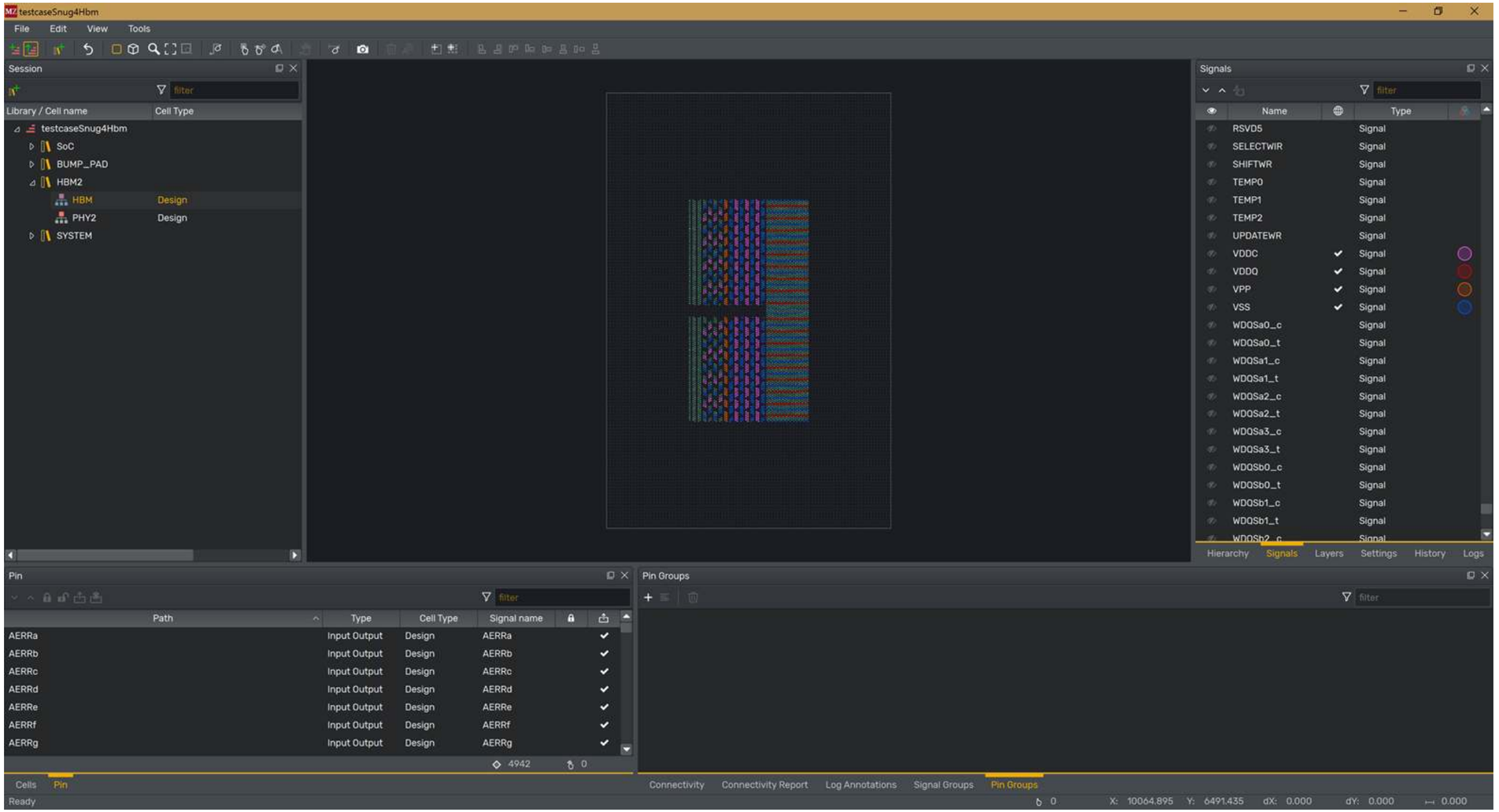
Hanoi

- Import from Physical Implementation
- Components Update
  - Logical, Physical
- Silicon Interposer Update
- Incremental I/O Planning
- Incremental Optimization
- Incremental Signal Assignment
- Export to Physical Implementation

Incremental Optimization

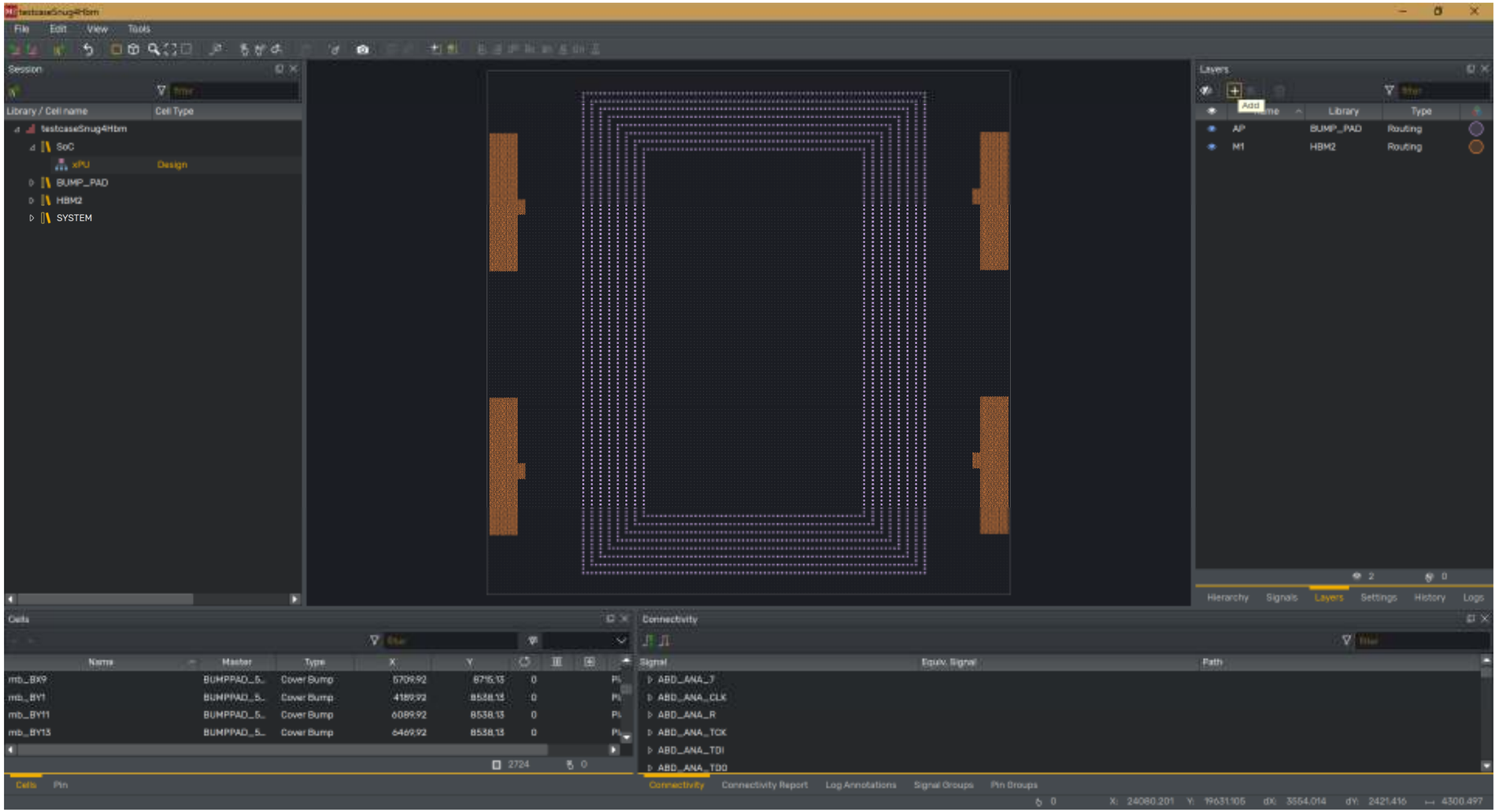
HBM Component Import

Excel/AIF Format Including Signal Assignment



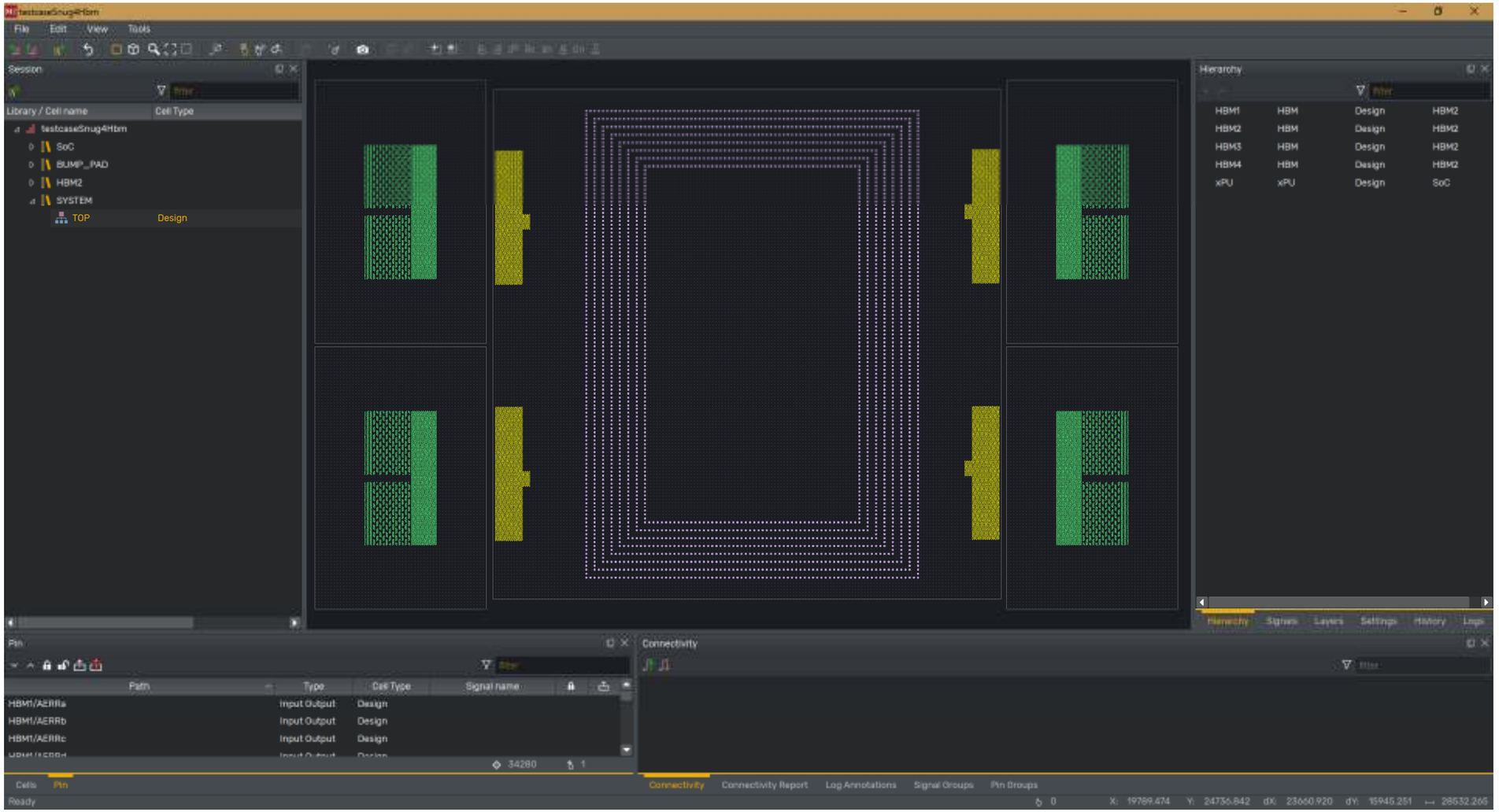
Processor Component Creation

Whiteboard Flow in HANOI



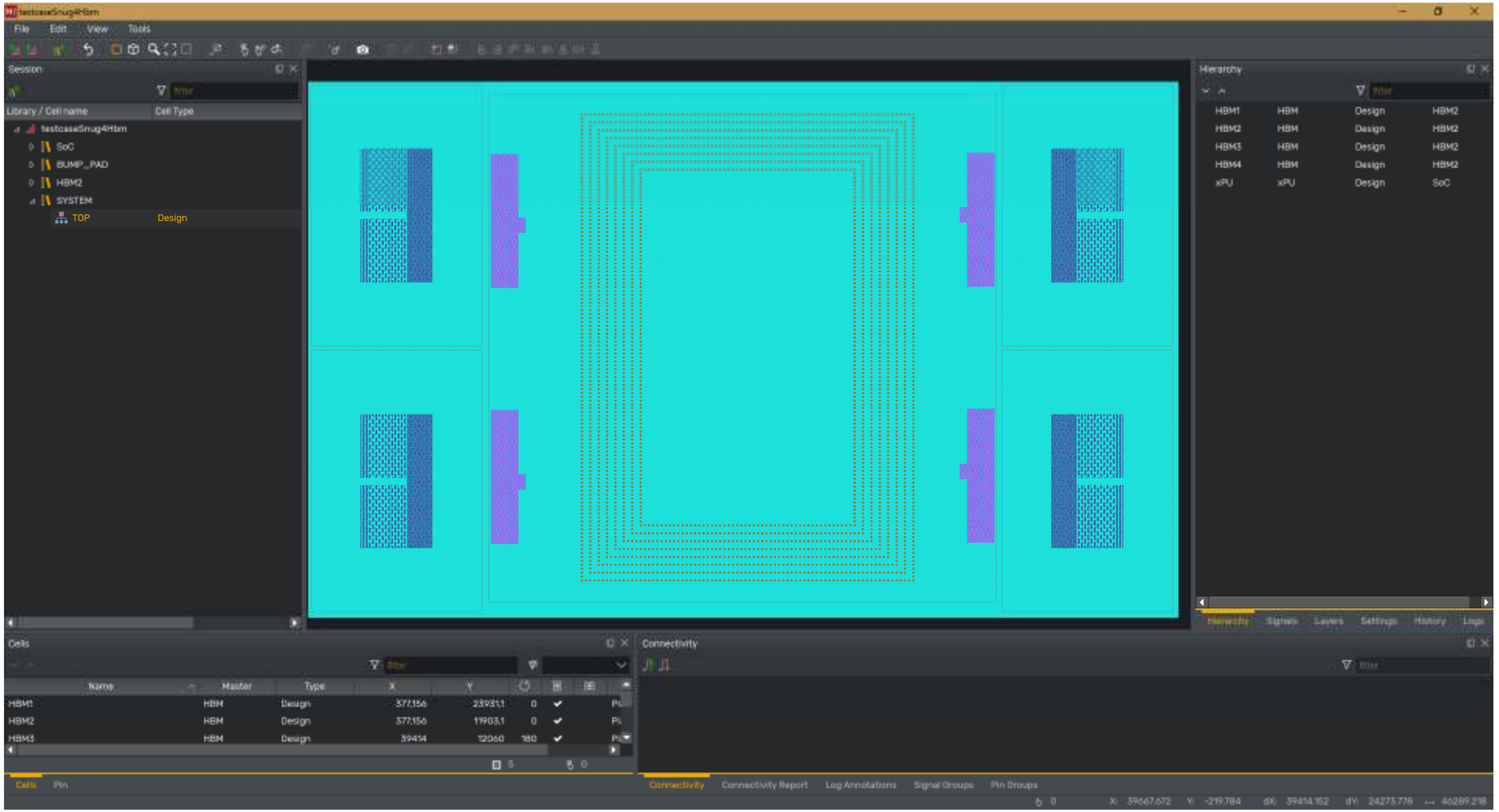
System Composition & Floorplanning

Alignment Functionalities Facilitate Placement



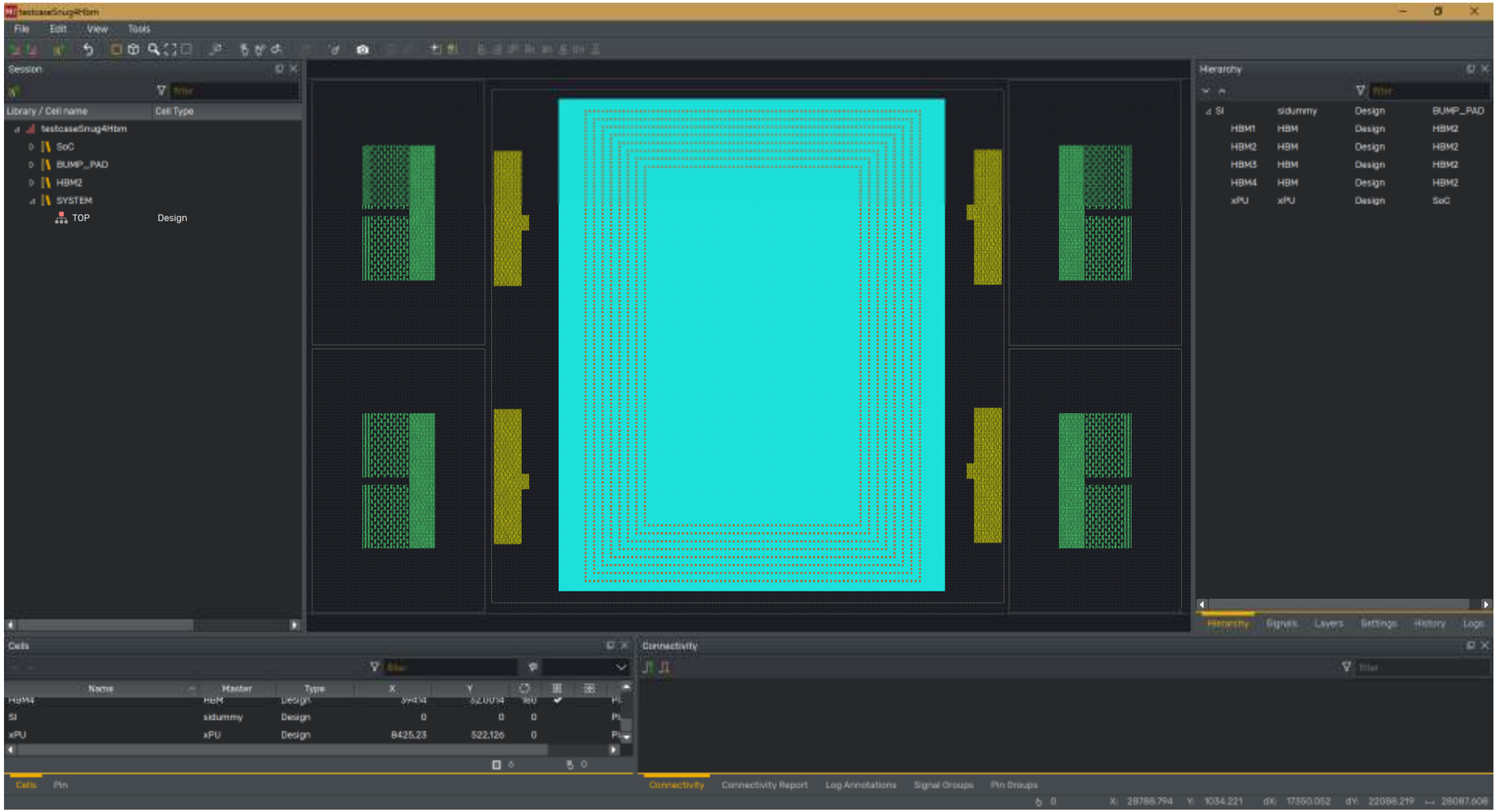
Silicon Interposer Creation

Boundary Definition



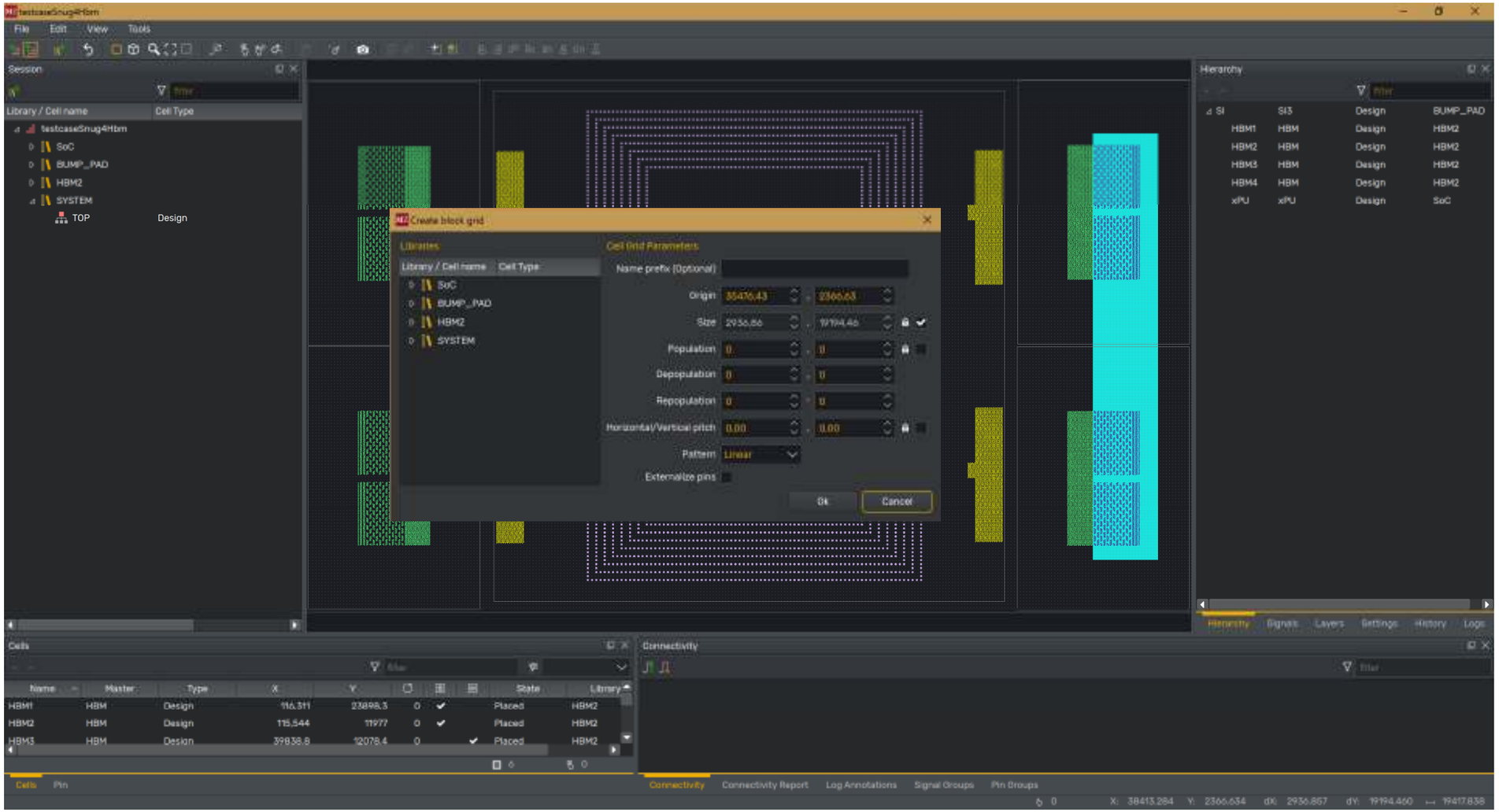
Silicon Interposer Creation

Multiple Bumping Areas Creation



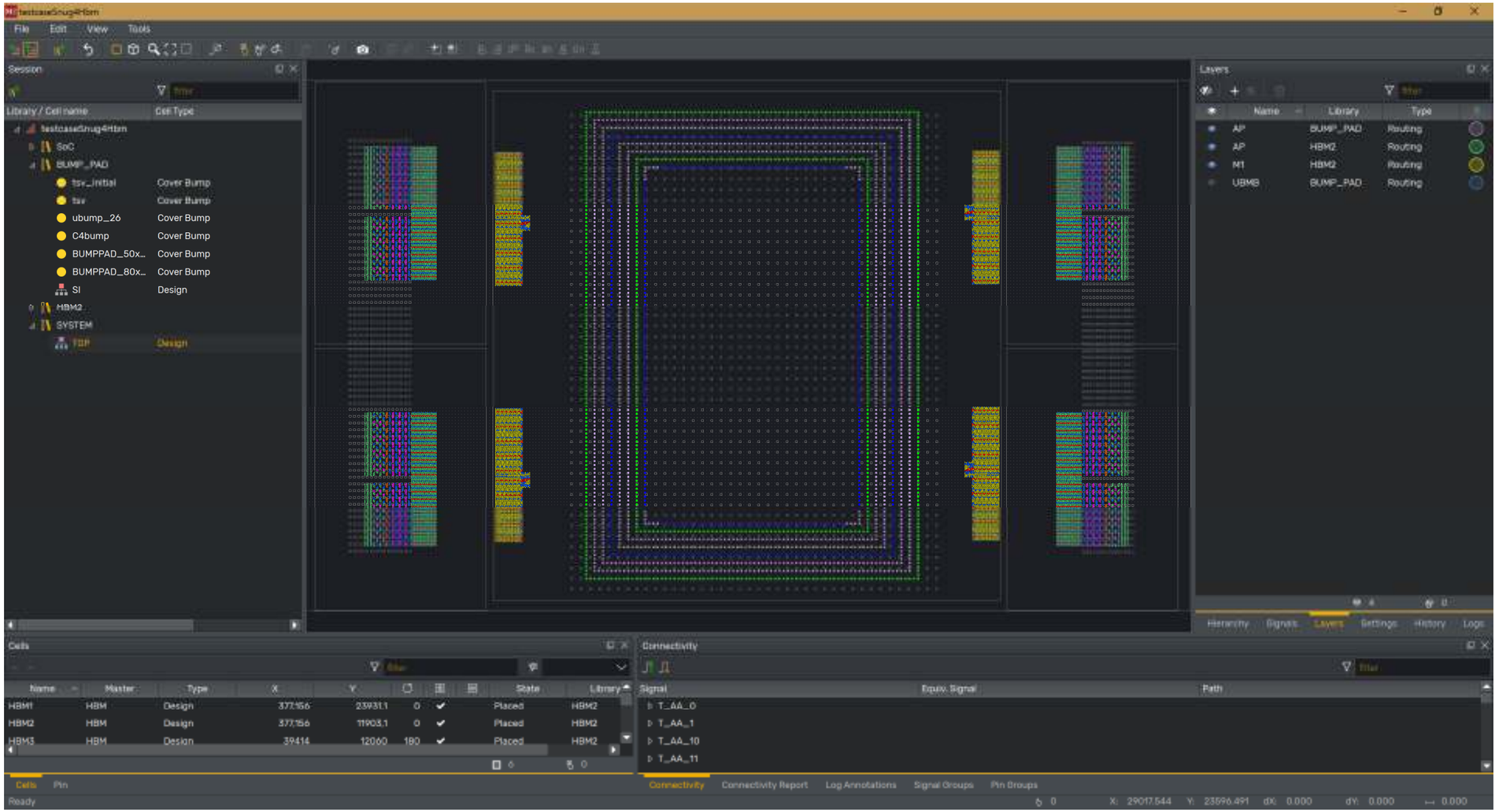
Silicon Interposer

Bumping Grid Definition by Number/Pitch/...



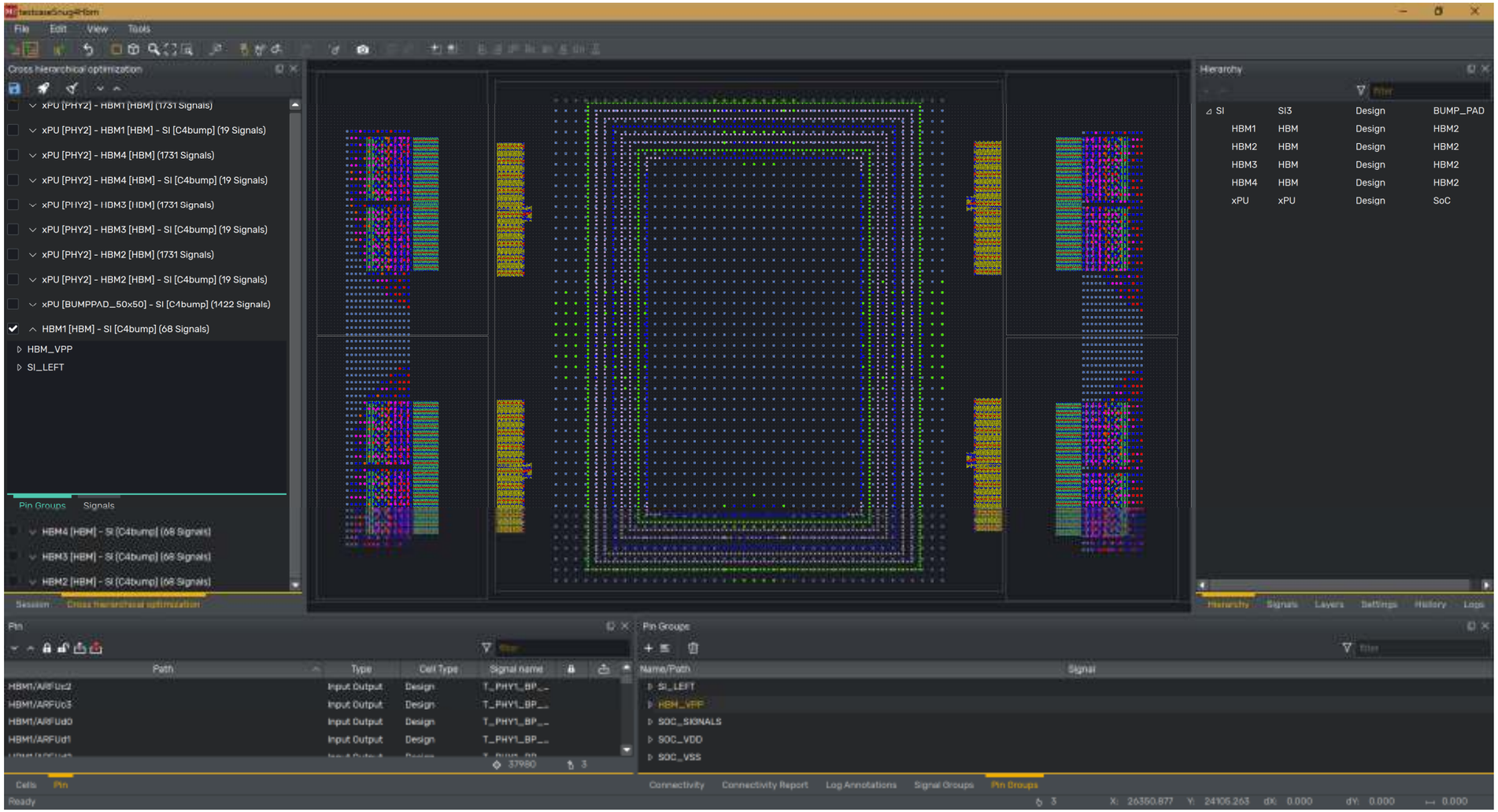
System Connectivity

Import from Verilog/csv and Global Signals Highlight



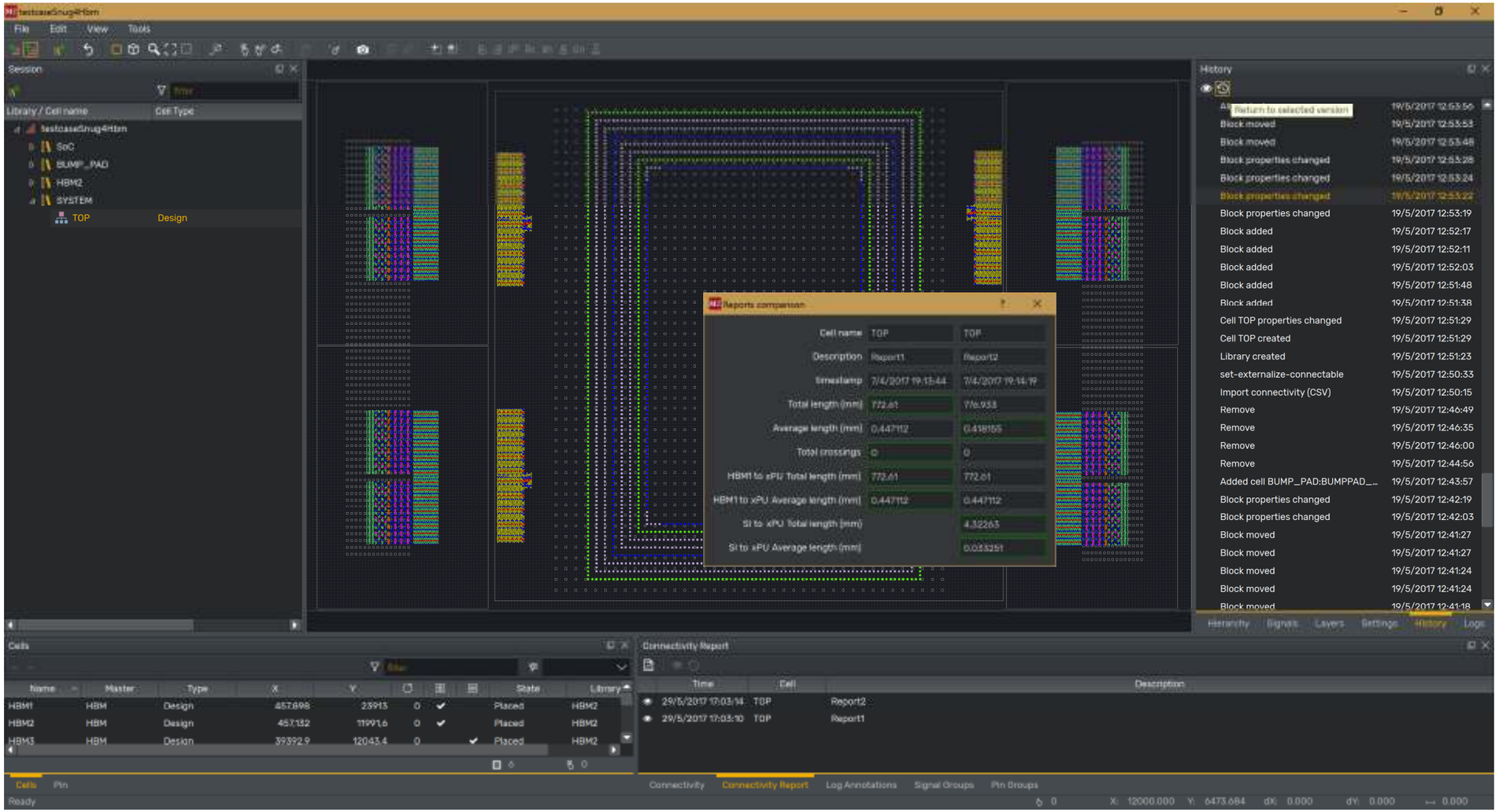
Cross Hierarchical Optimization

Signal & Pin Groups Driven: What & Where Approach



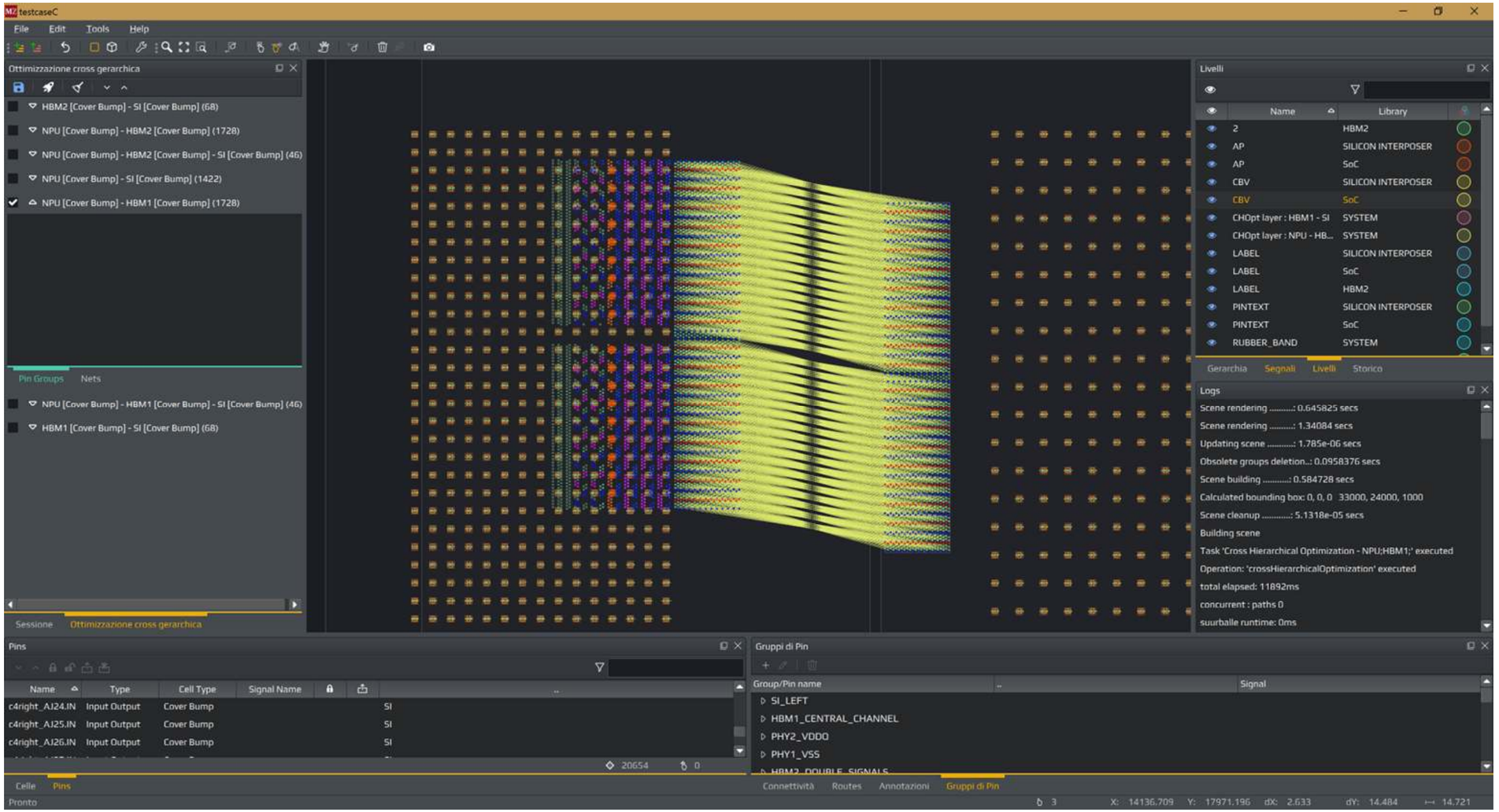
Time Machine Functionality

Report Generated on «Tagged» Versions



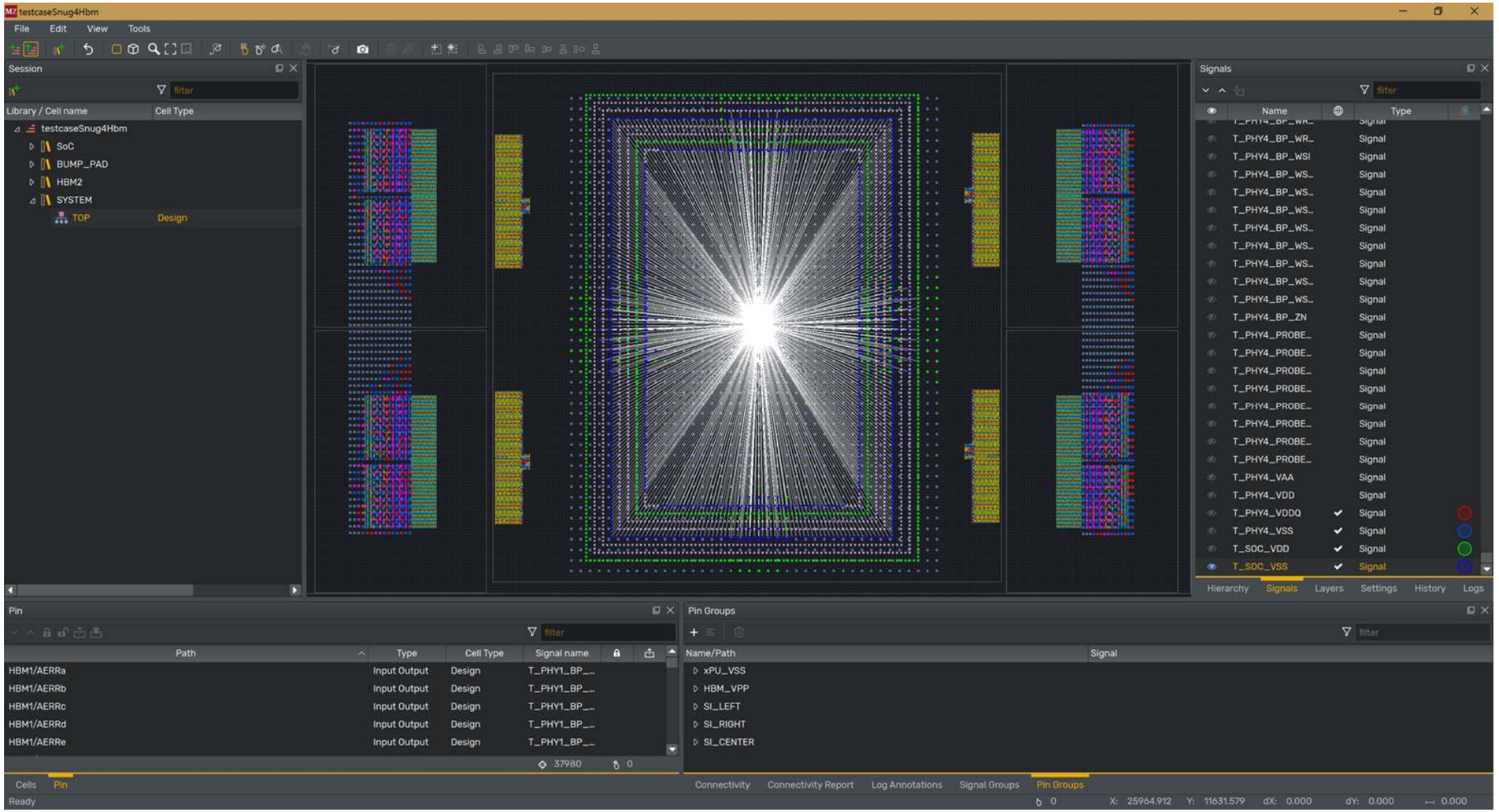
Fly-Lines Toggle For PHY-To-PHY Signals,...

Show & Hide Approach



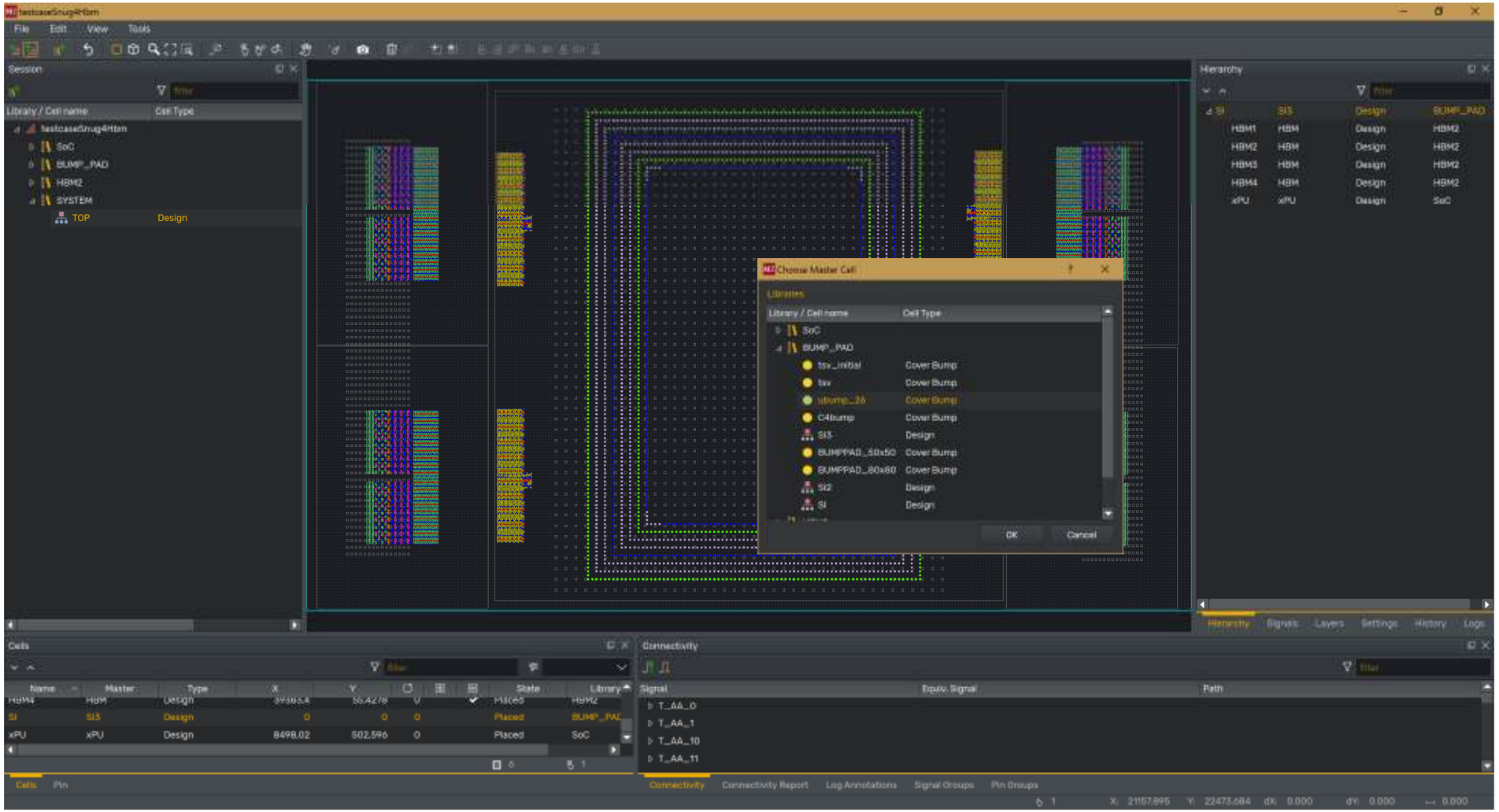
…And Global Signals

Show & Hide Approach



Automatic Creation Of Landing Pads

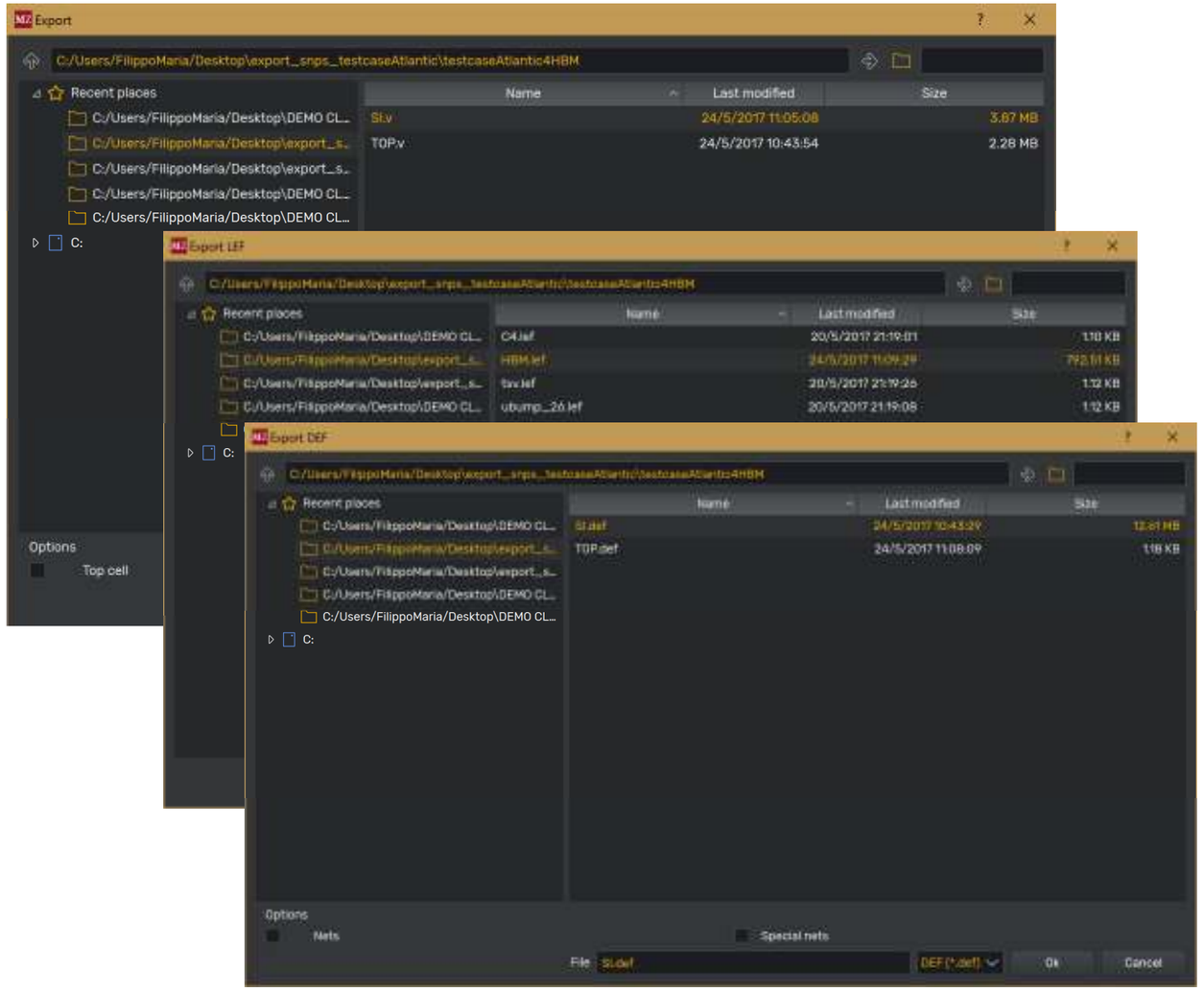
Mirroring of Microbumps on Silicon Interposer



Export To IC Compiler & Custom Compiler

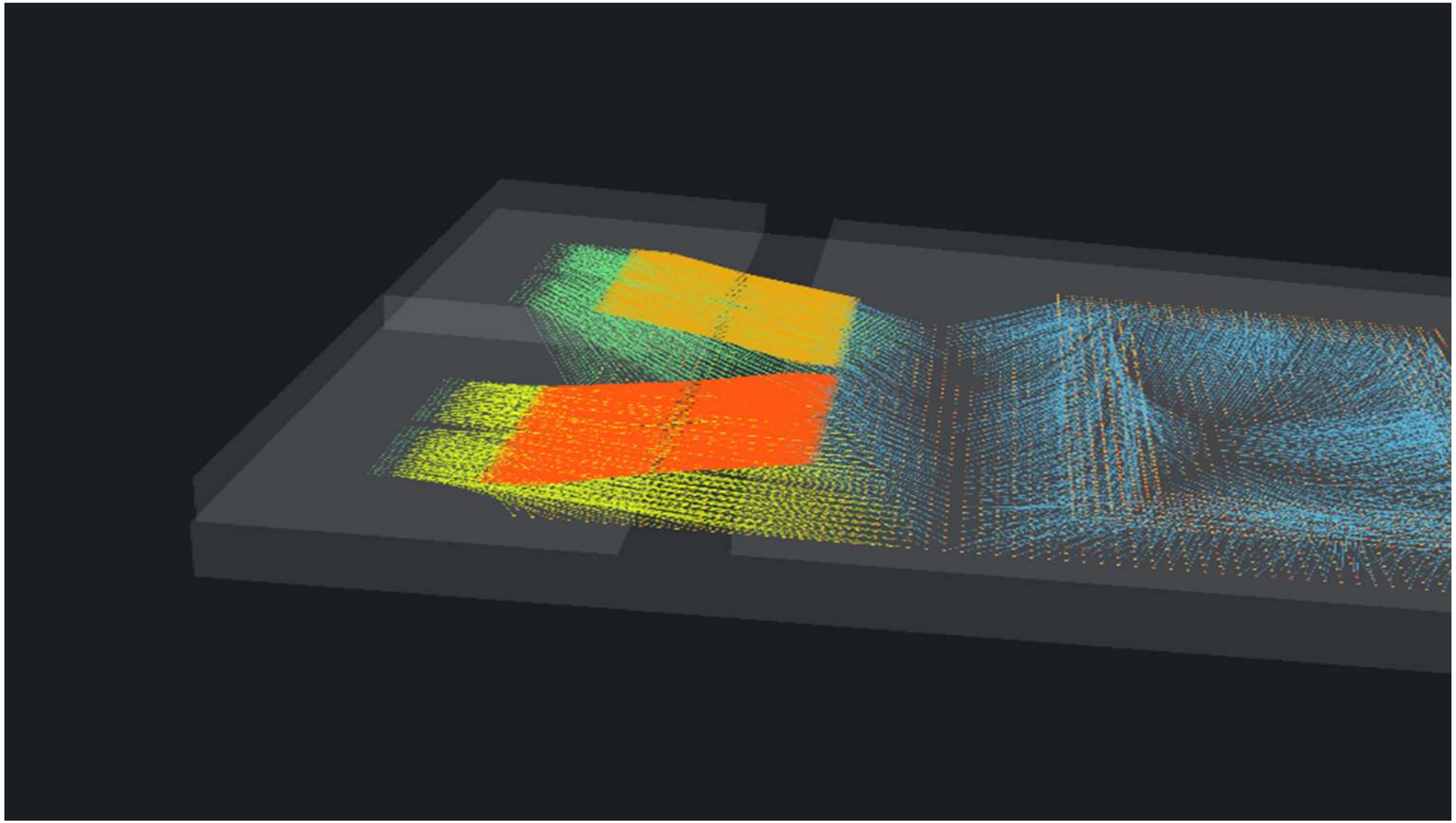
Regular vs. High-Speed Signals Routing Tools

- **Silicon Interposer** Routing
  - DEF + Verilog
    - Silicon Interposer Component
  - LEFs
    - Bumps (C4 e landing pad) and TSV
- **High Speed Signals** Routing
  - DEF + Verilog
    - TOP Level
  - LEFs
    - HBM & xPU



System 3D View

Detail of HBM-to-xPU-to-SI Fly-Line Connections



Conclusions

- **HANOI does provide a “whiteboard” flow to the rescue**
  - What exists can be imported, what doesn’t exist can be created from scratch
  - Many different configurations can be explored in a matter of hours
  - SI(s) interactively generated according to floorplan & design rules
  - Cross-hierarchical optimization enables overall best path-finding
  - Validated Roundtrip with IC Compiler

- **Industry only solution for package-silicon interposer-die co-design**
  - Common environment to represent **all** the levels of a 2.5D-IC design

- **There is much more to HANOI than 2.5D-IC !**

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Thanks!