



HANOI “Whiteboard” Flow The Seed For 2.5D-IC Implementation

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The Problem

Almost Nothing Exists, the Blackboard Is... White

- The processor (xPU) is in the flux
- The memories selection is still ongoing
- The silicon interposer(s) do(es) not exist – yes, there may be more than one !
- The package selection is a far future concern

- Yet, some “drawing” is critical to plan ahead
 - Complexity prevents “napkin and pencil” approaches
 - Thousands of signals, microbumps, TSV, C4, design-rules,...

- HANOI does provide a “whiteboard” flow to the rescue
 - What exists can be imported, what doesn't exist can be created from scratch

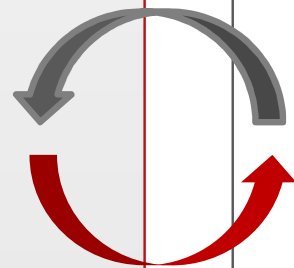
HANOI “Whiteboard” Flow

The Seed for 2.5D-IC Physical Implementation

hanoi

Early Exploration

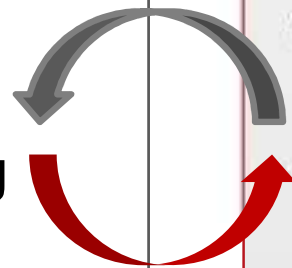
- Components Import
 - HBM, Package,...
- Components Creation
 - xPU,...
- System Floorplanning
- Silicon Interposer Creation
 - TSV, C4,...
 - [Partial] Connectivity,...
- I/O Planning
- Cross-Hierarchical Optimization
- Signal Assignment
- Export to Physical Implementation



Physical Implementation (Third Party Tools)

System floorplanning
Physical Implementation
xPU,...

Silicon Interposer Routing
PHY-to-PHY
Microbump-to-TSV
TSV-to-C4



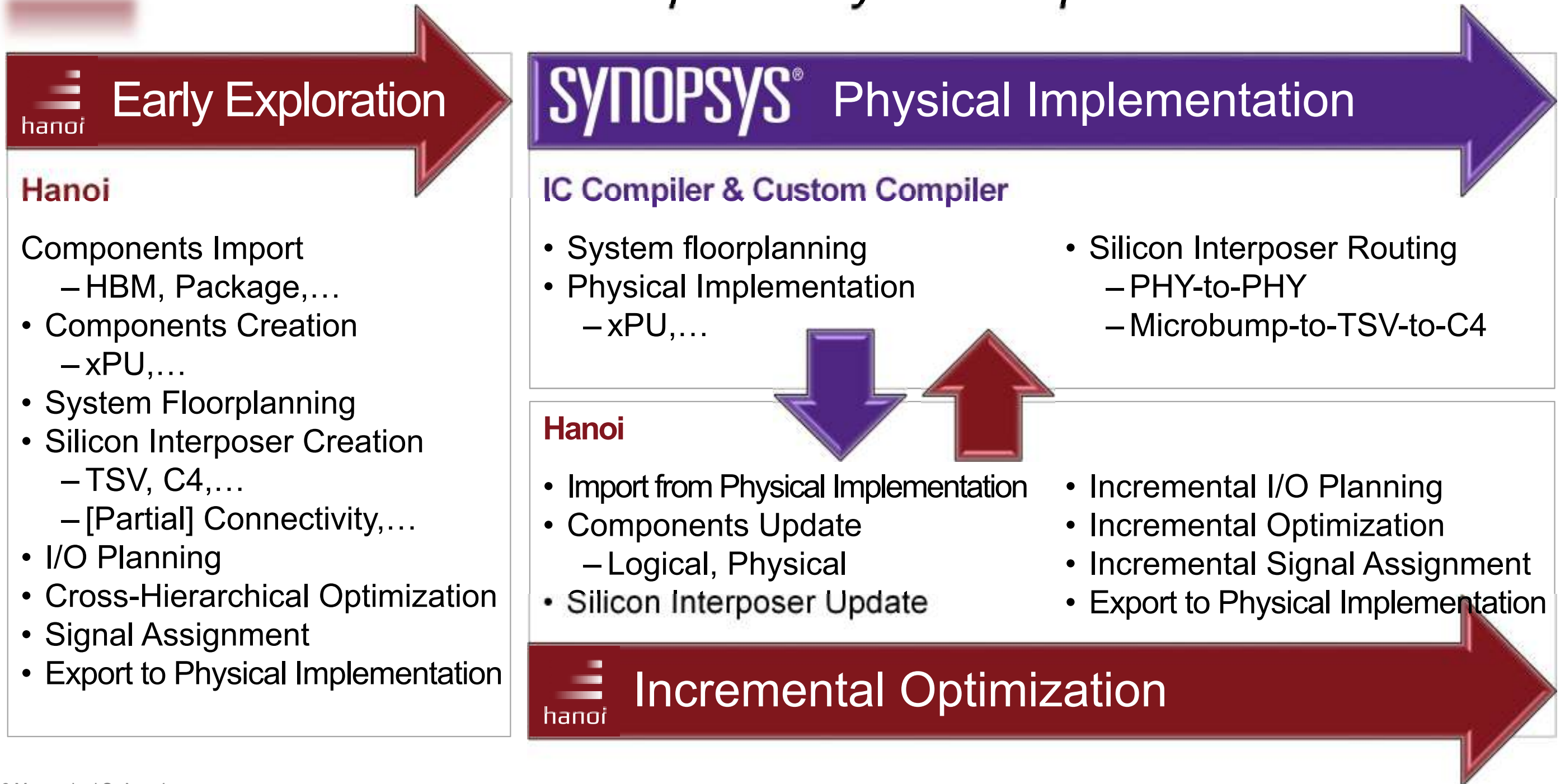
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Incremental Optimization

- Import from Physical Implementation
- Components Update
 - Logical, Physical
- Silicon Interposer Update
- Incremental I/O Planning
- Incremental Optimization
- Incremental Signal Assignment
- Export to Physical Implementation

HANOI “Whiteboard” Flow

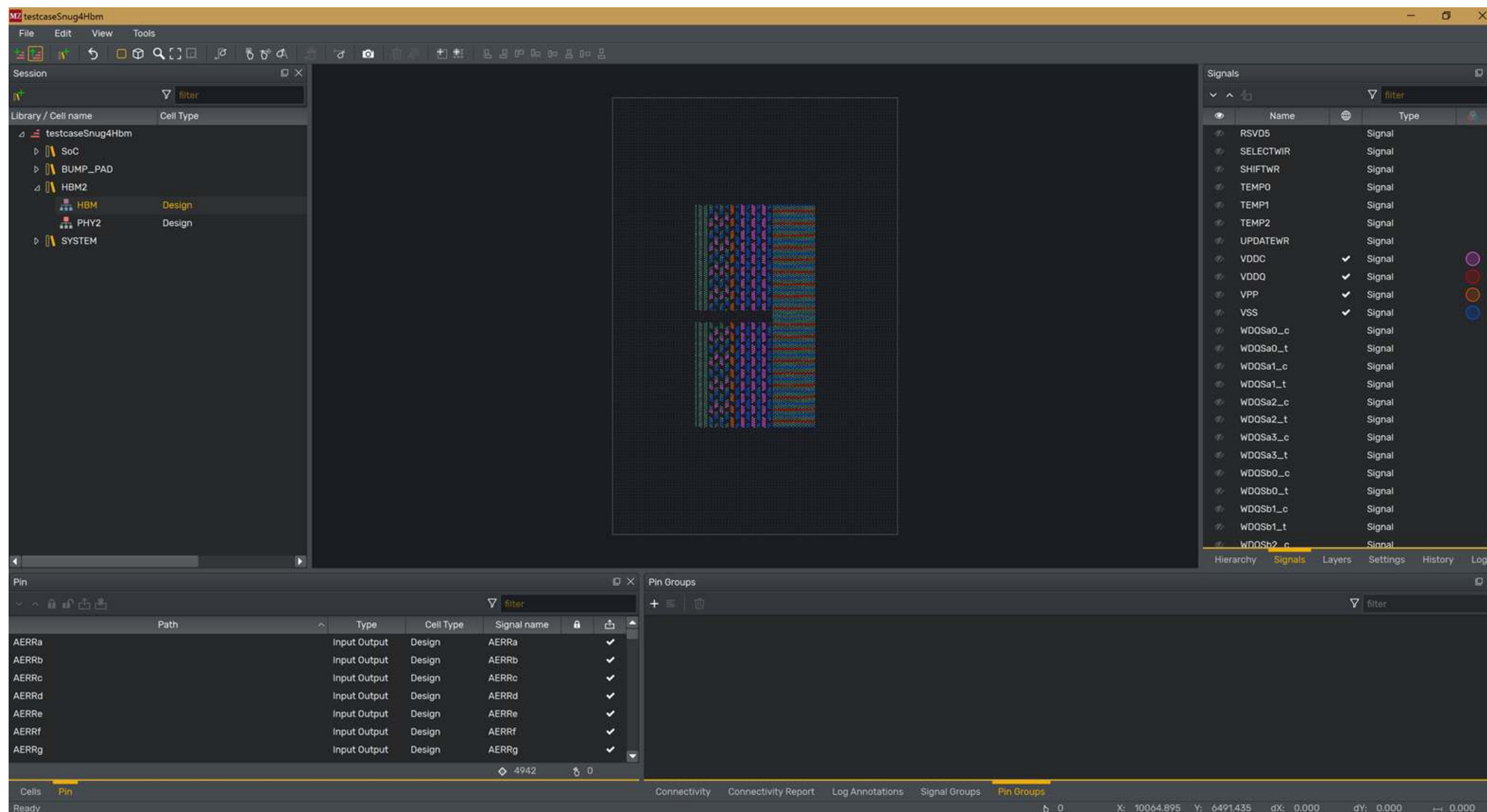
The Seed for IC Compiler Physical Implementation





HBM Component Import

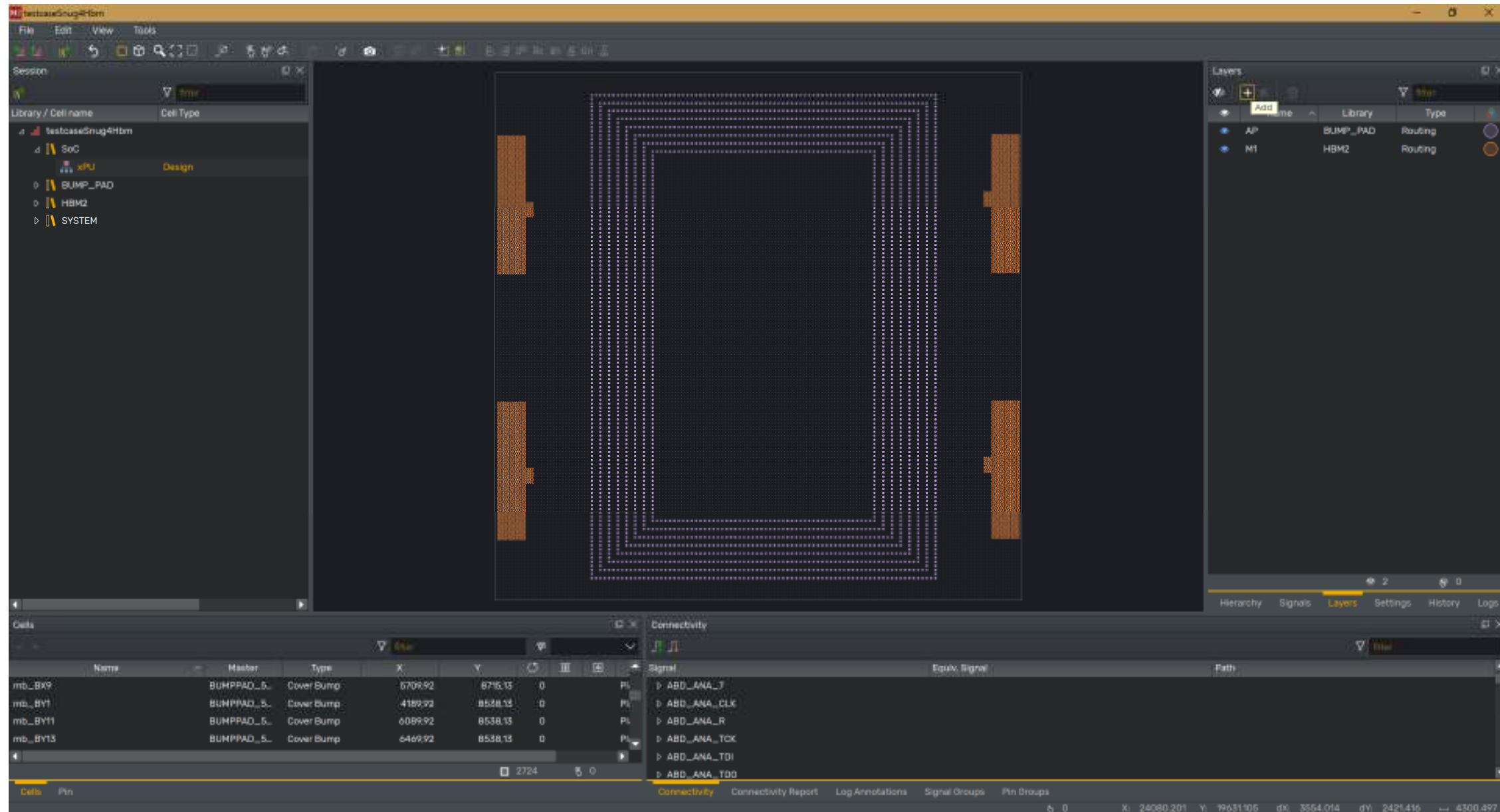
Excel/AIF Format Including Signal Assignment





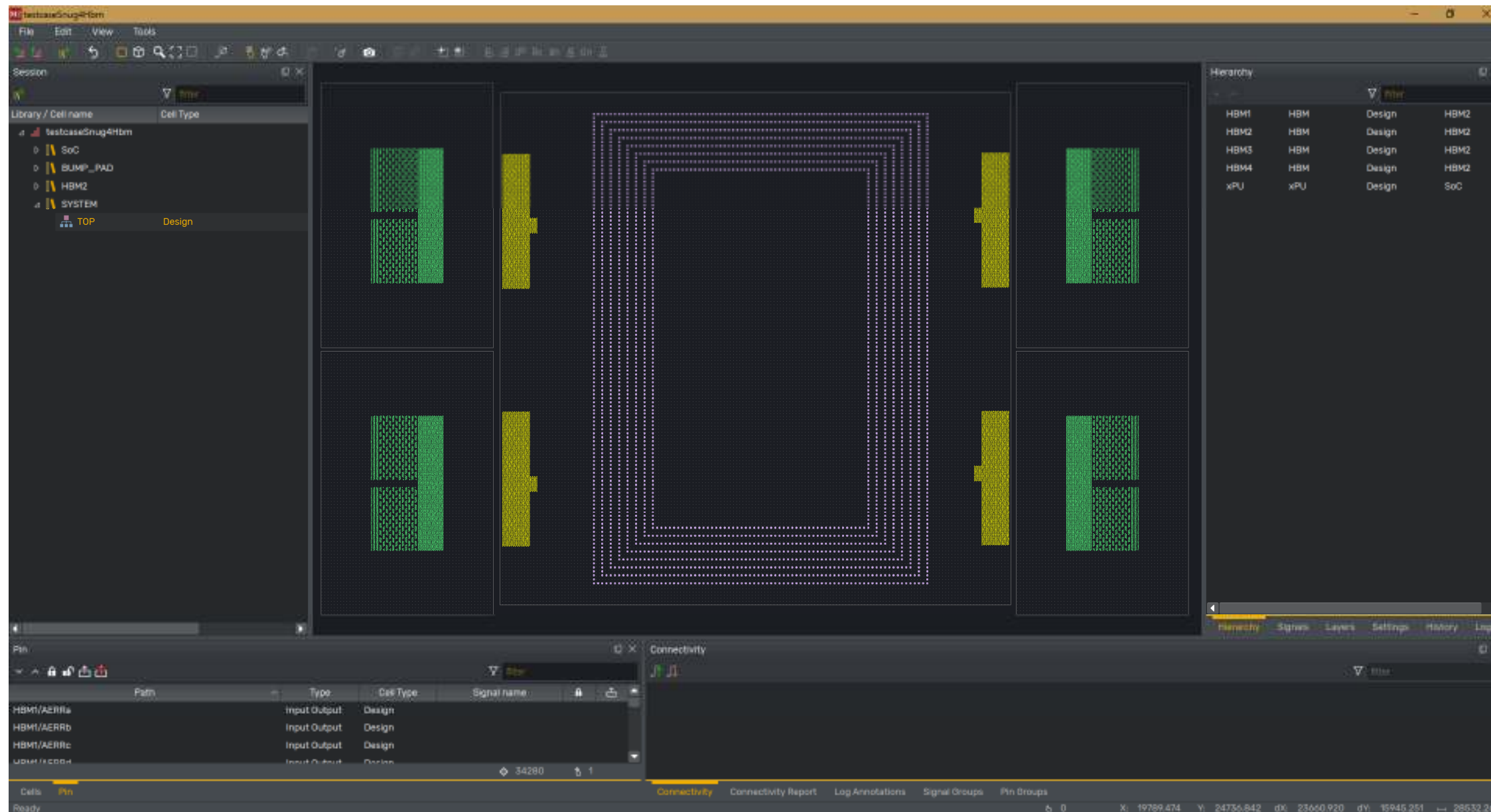
Processor Component Creation

Whiteboard Flow in HANOI



System Composition & Floorplanning

Alignment Functionalities Facilitate Placement





Silicon Interposer Creation

Boundary Definition

The screenshot shows a CAD software interface for silicon interposer creation. The main workspace displays a cyan-colored interposer with a central orange dashed-line boundary. The interface includes a left sidebar with a library tree, a right sidebar with a hierarchy table, and a bottom status bar with a connectivity table.

Library / Cell name

- testcaseSnug4Hbm
 - SoC
 - BUMP_PAD
 - HBM2
 - SYSTEM
 - TOP

Hierarchy

Cell Name	Parent	Type	Sub-Cell
HBM1	HBM	Design	HBM2
HBM2	HBM	Design	HBM2
HBM3	HBM	Design	HBM2
HBM4	HBM	Design	HBM2
xPU	xPU	Design	SoC

Cells

Name	Master	Type	X	Y	W	H	Pin
HBM1	HBM	Design	377156	239311	0	0	P0
HBM2	HBM	Design	377156	199031	0	0	P1
HBM3	HBM	Design	39414	12060	180	0	P10

Connectivity

Cell	Pin	Value
HBM1	P0	0
HBM2	P1	0
HBM3	P10	0

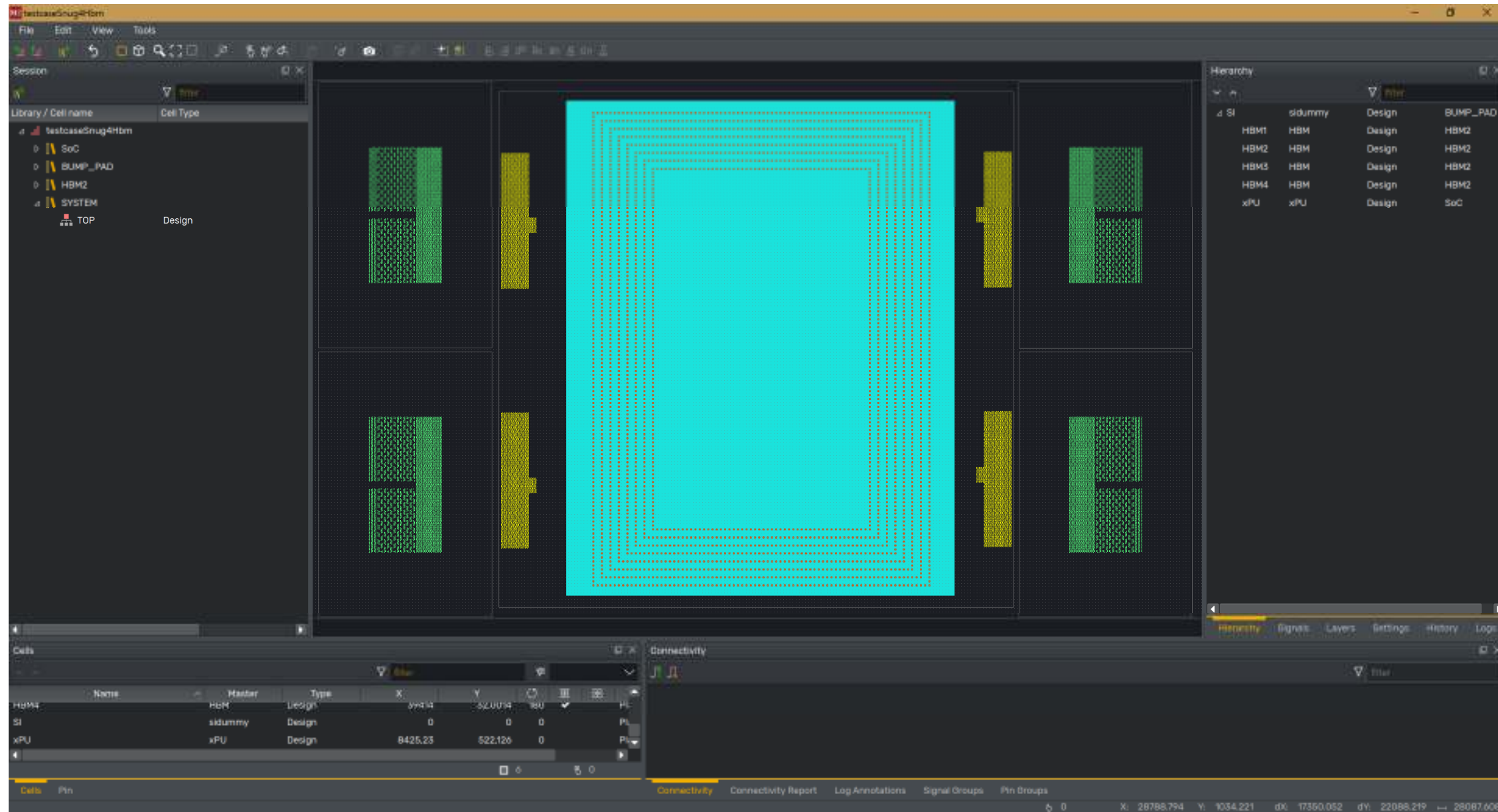
Status Bar

X: 39667.672 Y: -219.784 dx: 39414.162 dy: 24273.778 45289.218



Silicon Interposer Creation

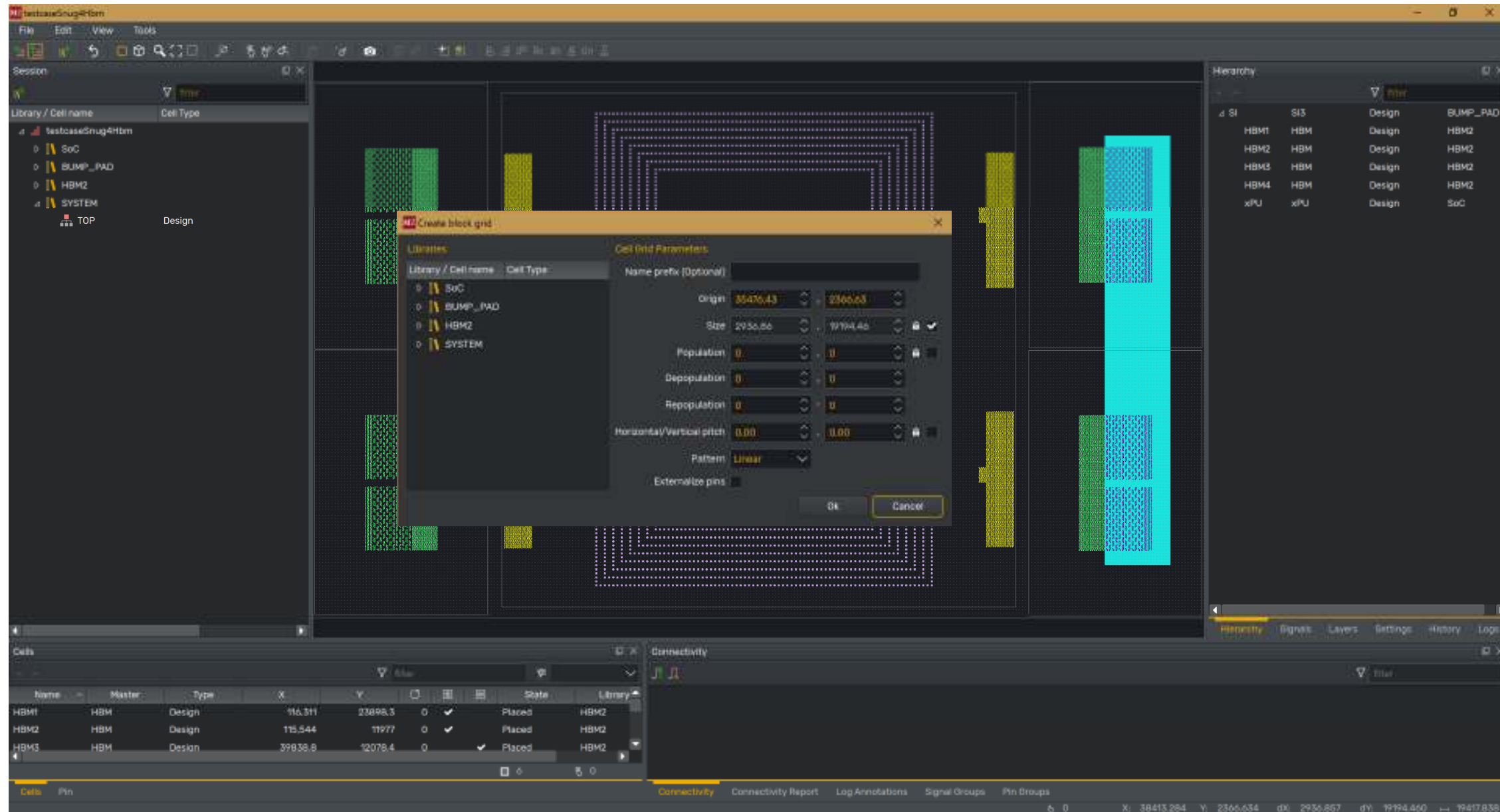
Multiple Bumping Areas Creation





Silicon Interposer

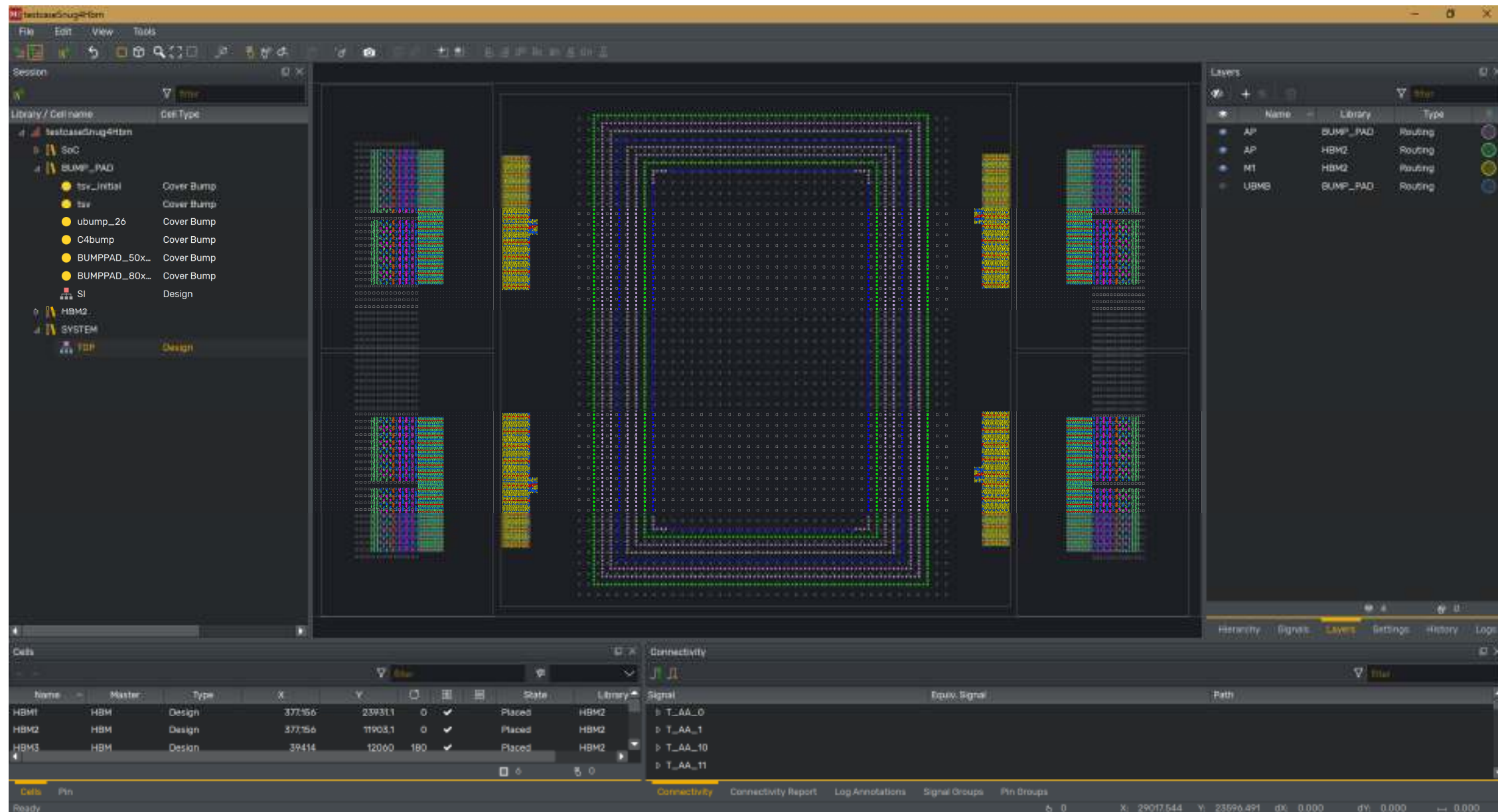
Bumping Grid Definition by Number/Pitch/...





System Connectivity

Import from Verilog/csv and Global Signals Highlight



Cross Hierarchical Optimization

Signal & Pin Groups Driven: What & Where Approach

The screenshot displays a PCB design tool interface for cross-hierarchical optimization. The main workspace shows a grid of the board layout with various signal paths highlighted in different colors (blue, green, yellow, red). The left sidebar contains a tree view of signal groups, with 'HBM1 [HBM] - SI [C4bump] (68 Signals)' selected. The right sidebar shows a hierarchy table with columns for component name, type, and location. The bottom panel shows a detailed view of pin groups, including a table with columns for Path, Type, Cell Type, and Signal name.

Path	Type	Cell Type	Signal name
HBM1/ARF0c2	Input Output	Design	T_PHY1_BP_...
HBM1/ARF0c3	Input Output	Design	T_PHY1_BP_...
HBM1/ARF0d0	Input Output	Design	T_PHY1_BP_...
HBM1/ARF0d1	Input Output	Design	T_PHY1_BP_...
HBM1/ARF0d2	Input Output	Design	T_PHY1_BP_...
			37980

Component	Type	Location	Signal
SI	SI3	Design	BUMP_PAD
HBM1	HBM	Design	HBM2
HBM2	HBM	Design	HBM2
HBM3	HBM	Design	HBM2
HBM4	HBM	Design	HBM2
xPU	xPU	Design	SoC

Time Machine Functionality

Report Generated on «Tagged» Versions

The screenshot displays a PCB design software interface with a connectivity report window open. The report compares two versions of a cell named 'TOP'.

Cell name	TOP	TOP
Description	Report1	Report2
Timestamp	7/4/2017 19:15:44	7/4/2017 19:14:17
Total length (mm)	772.61	776.958
Average length (mm)	0.447112	0.418105
Total crossings	0	0
HBM1 to xPU Total length (mm)	772.61	772.61
HBM1 to xPU Average length (mm)	0.447112	0.447112
SI to xPU Total length (mm)		4.32263
SI to xPU Average length (mm)		0.025251

The background shows a PCB layout with various components and a history log on the right side of the interface.

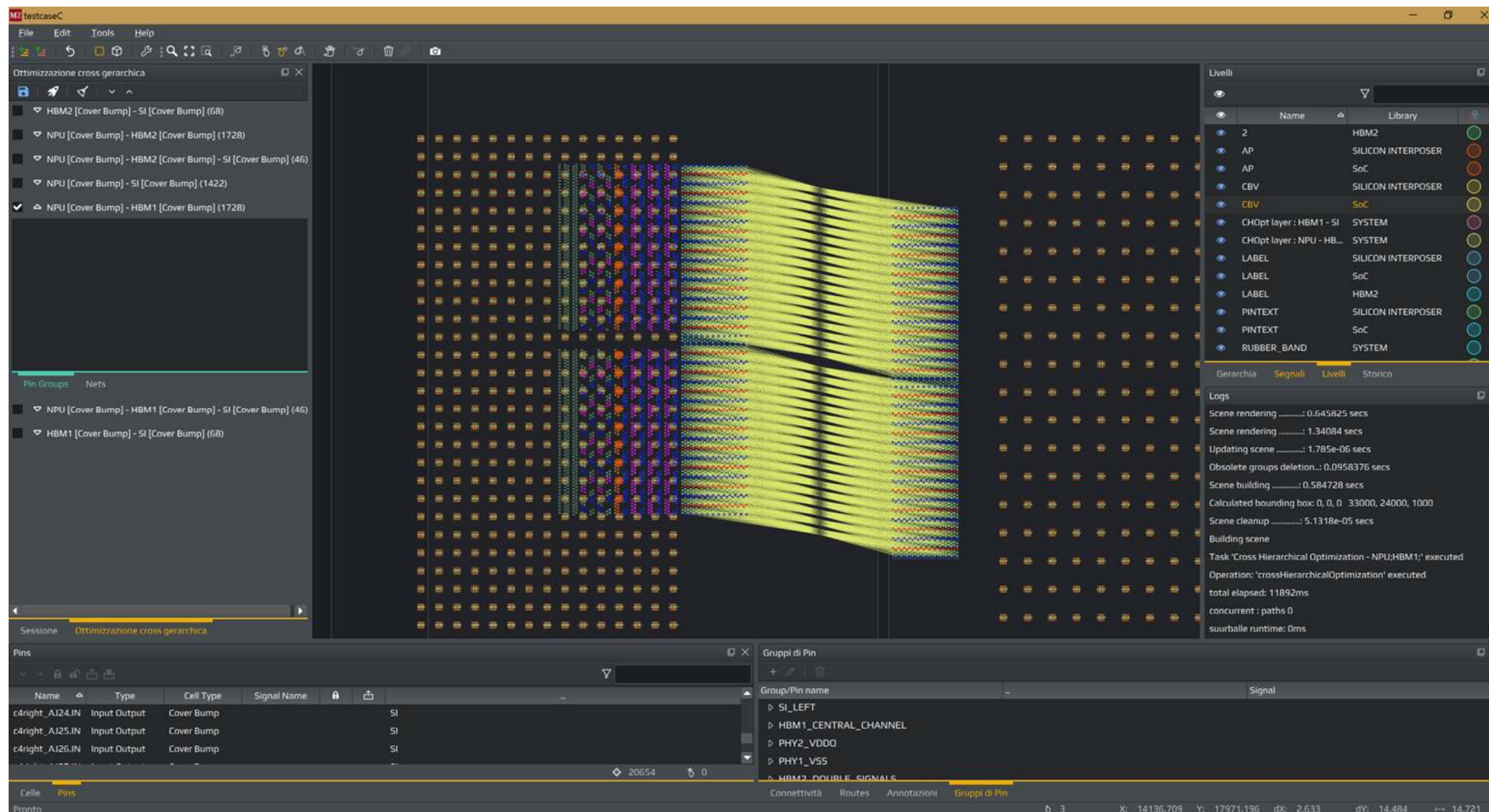
History	Timestamp
Return to selected version	19/5/2017 12:53:59
Block moved	19/5/2017 12:53:53
Block moved	19/5/2017 12:53:48
Block properties changed	19/5/2017 12:53:28
Block properties changed	19/5/2017 12:53:24
Block properties changed	19/5/2017 12:53:22
Block properties changed	19/5/2017 12:53:19
Block added	19/5/2017 12:52:17
Block added	19/5/2017 12:52:11
Block added	19/5/2017 12:52:03
Block added	19/5/2017 12:51:48
Block added	19/5/2017 12:51:38
Cell TOP properties changed	19/5/2017 12:51:29
Cell TOP created	19/5/2017 12:51:29
Library created	19/5/2017 12:51:23
set-externalize-connectable	19/5/2017 12:50:33
Import connectivity (CSV)	19/5/2017 12:50:15
Remove	19/5/2017 12:46:49
Remove	19/5/2017 12:46:35
Remove	19/5/2017 12:46:00
Remove	19/5/2017 12:44:56
Added cell BUMP_PAD:BUMPPAD_...	19/5/2017 12:43:57
Block properties changed	19/5/2017 12:42:19
Block properties changed	19/5/2017 12:42:03
Block moved	19/5/2017 12:41:27
Block moved	19/5/2017 12:41:24
Block moved	19/5/2017 12:41:24
Block moved	19/5/2017 12:41:24
Block moved	19/5/2017 12:41:18

At the bottom, a 'Connectivity Report' table is visible:

Time	Cell	Description
29/5/2017 17:03:14	TOP	Report2
29/5/2017 17:03:10	TOP	Report1

Fly-Lines Toggle For PHY-To-PHY Signals,...

Show & Hide Approach





...And Global Signals *Show & Hide Approach*

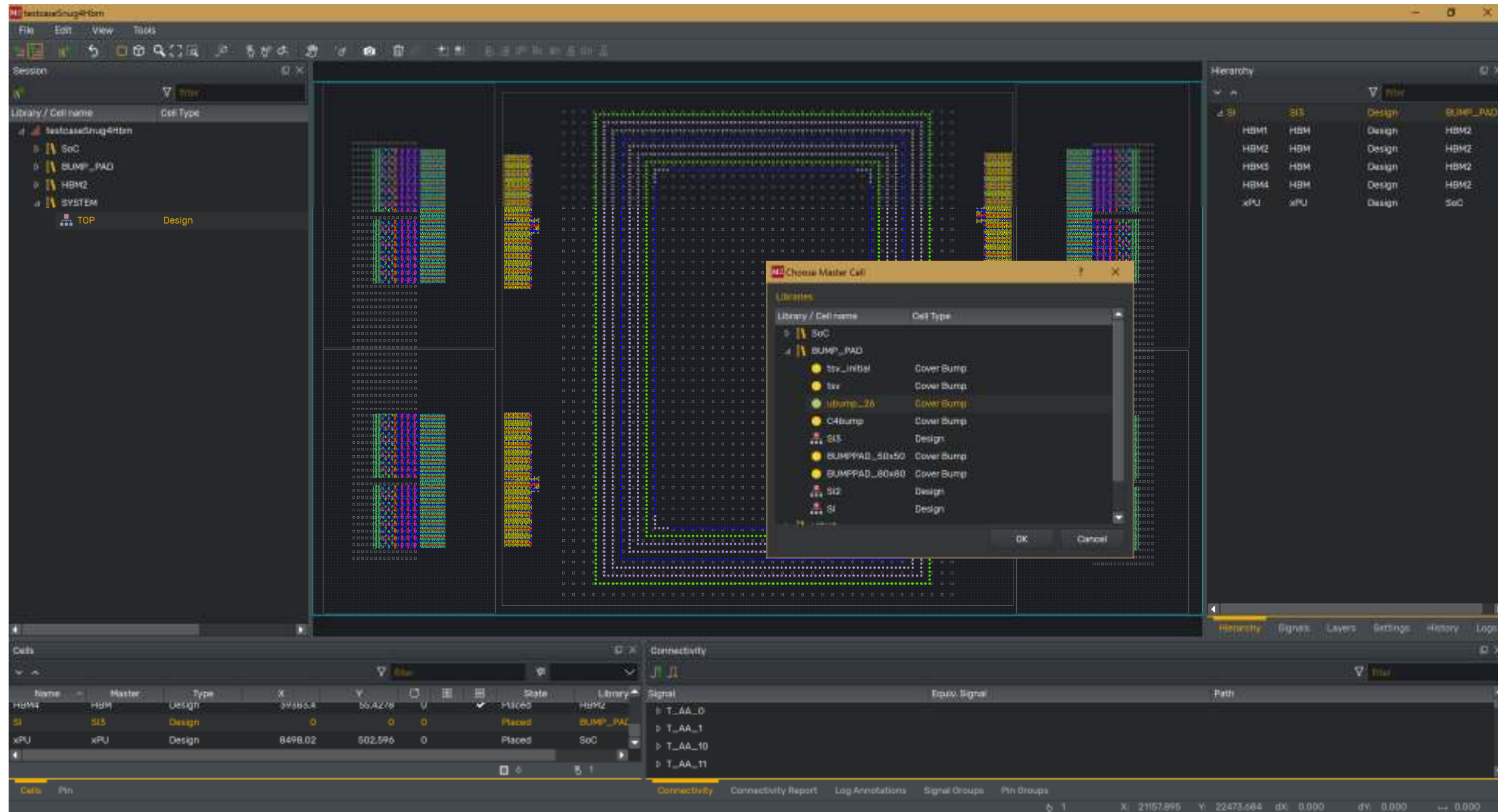
The screenshot displays a design tool interface for a project named 'testcaseSnug4Hbm'. The main workspace shows a complex circuit diagram with a central starburst pattern of connections. The interface includes several panes:

- Library / Cell name:** Shows a hierarchy of components: testcaseSnug4Hbm, SoC, BUMP_PAD, HBM2, SYSTEM, and TOP (Design).
- Signals:** A list of signals with columns for Name, Type, and visibility. Signals include T_PHY4_BP_WR_, T_PHY4_BP_WSI, T_PHY4_BP_WS_, T_PHY4_BP_WS_ (multiple instances), T_PHY4_BP_ZN, T_PHY4_PROBE_ (multiple instances), T_PHY4_VAA, T_PHY4_VDD, T_PHY4_VDDQ, T_PHY4_VSS, T_SOC_VDD, and T_SOC_VSS.
- Pin:** A table listing pins with columns for Path, Type, Cell Type, and Signal name. The table shows five pins (HBM1/AERRa through HBM1/AERRe) all of type 'Input Output' and 'Design', with signal names starting with 'T_PHY1_BP_'. The total count is 37980 pins.
- Pin Groups:** A list of pin groups including xPU_VSS, HBM_VPP, SI_LEFT, SI_RIGHT, and SI_CENTER.

The bottom status bar shows coordinates (X: 25964.912, Y: 11631.579) and zoom level (0.000).

Automatic Creation Of Landing Pads

Mirroring of Microbumps on Silicon Interposer



Export To IC Compiler & Custom Compiler

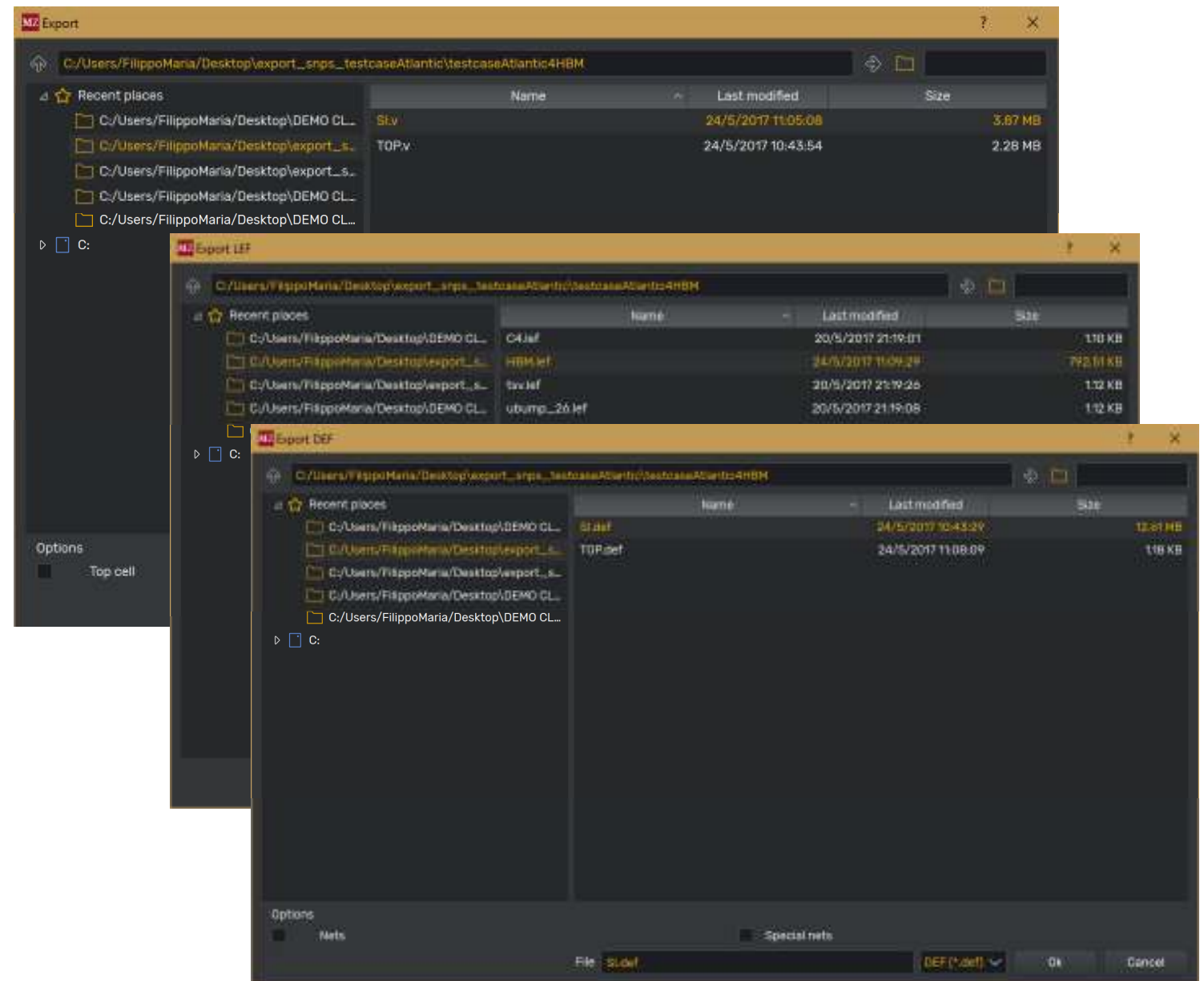
Regular vs. High-Speed Signals Routing Tools

- **Silicon Interposer Routing**

- DEF + Verilog
- Silicon Interposer Component
- LEFs
- Bumps (C4 e landing pad) and TSV

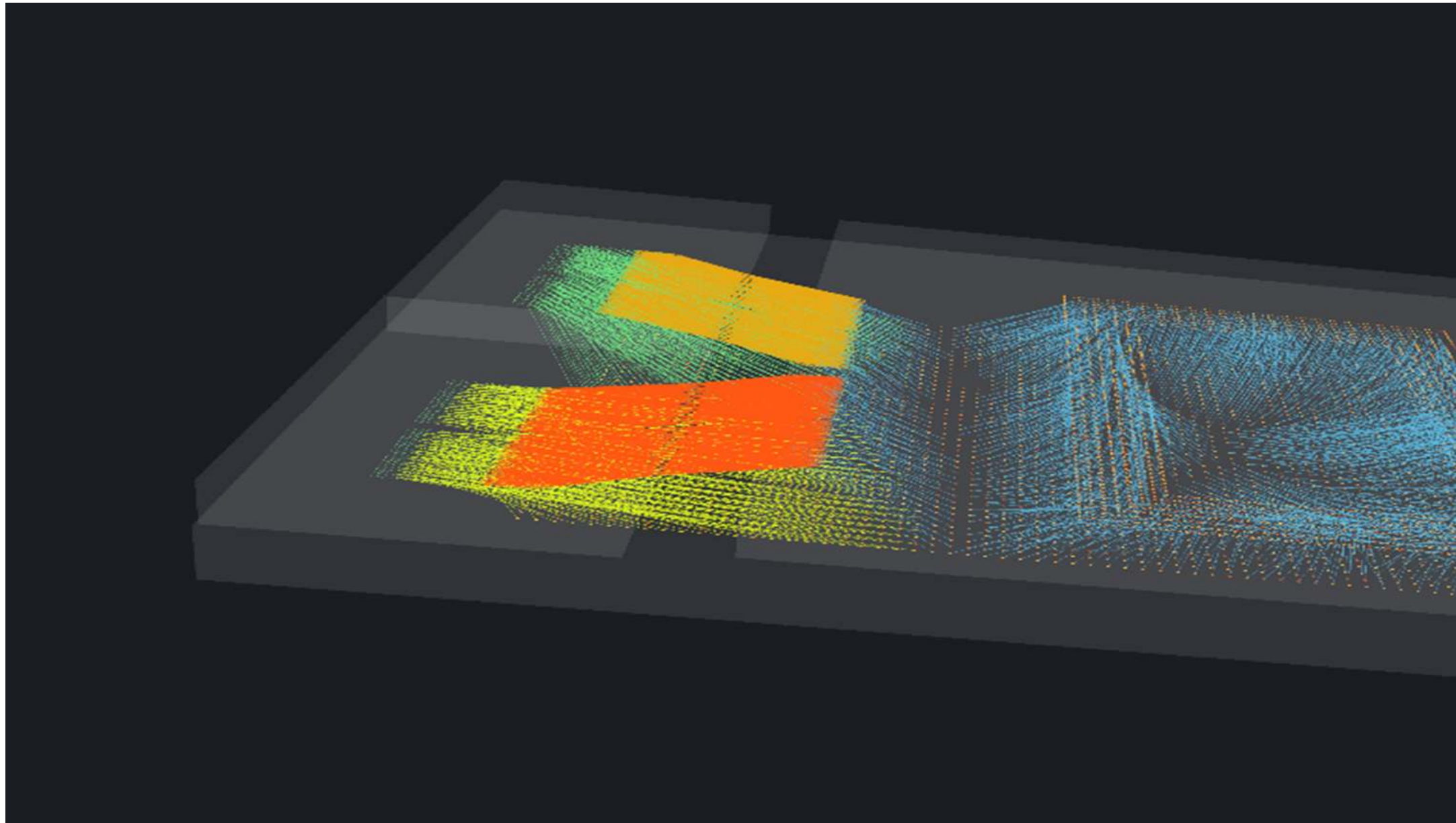
- **High Speed Signals Routing**

- DEF + Verilog
- TOP Level
- LEFs
- HBM & xPU



System 3D View

Detail of HBM-to-xPU-to-SI Fly-Line Connections



- **HANOI does provide a “whiteboard” flow to the rescue**
 - What exists can be imported, what doesn't exist can be created from scratch
 - Many different configurations can be explored in a matter of hours
 - SI(s) interactively generated according to floorplan & design rules
 - Cross-hierarchical optimization enables overall best path-finding
 - Validated Roundtrip with IC Compiler
- **Industry only solution for package-silicon interposer-die co-design**
 - Common environment to represent all the levels of a 2.5D-IC design
- **There is much more to HANOI than 2.5D-IC !**



Thanks!

